

FIG. 1 PRIOR ART

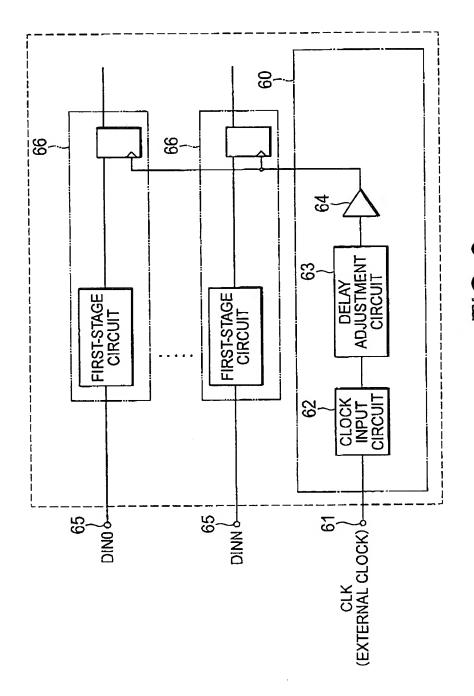
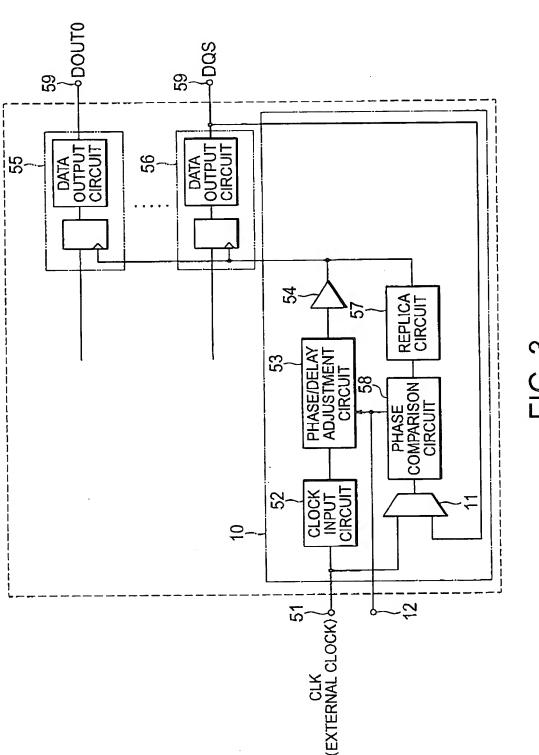
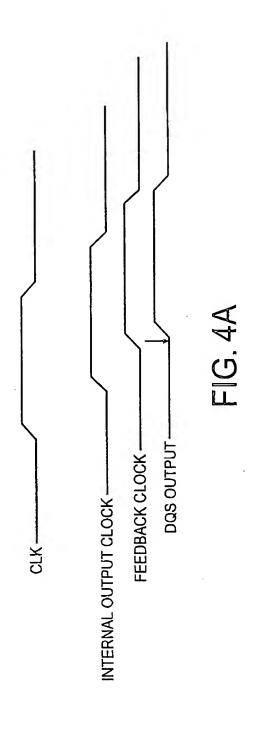


FIG. 2 PRIOR ART







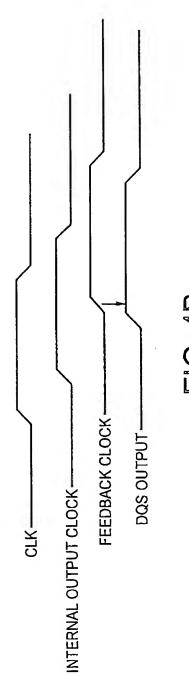


FIG. 4B

30 99 99 FIG. 5 DELAY H ADJUSTMENT I CIRCUIT -32 63 FIRST-STAGE CIRCUIT FIRST-STAGE CIRCUIT FIRST-STAGE CIRCUIT CLOCK INPUT CIRCUIT 34 65 65 6 DINO &

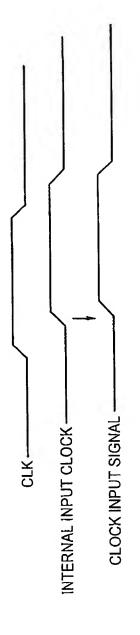
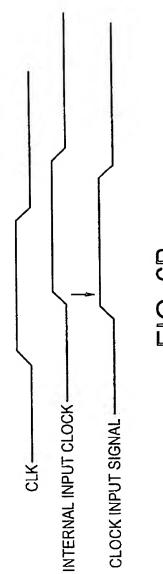


FIG. 6A



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FIG. 6B